PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application. No: 10/055,691
Filed: October 29, 2001
Inventor(s):
Hugo A. Andrade, Brian Keith Odom, Cary Paul Butler, Joseph E. Peck and Newton G. Petersen
Title: SYSTEM AND METHOD FOR DEBUGGING A SOFTWARE PROGRAM

§

Examiner: Steelman, Mary J.
Group/Art Unit: 2191
Atty. Dkt. No: 5150-63400

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date indicated below.

Jeffrey C. Hood

Signature

8/3/2005
Date

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant requests consideration of ☒ the references listed on the attached Form PTO-1449 and/or ☐ the additional information identified below in paragraph 3. A copy of each reference C1–C67 listed on the Form PTO-1449 was previously submitted on January 3, 2005.

1. This Information Disclosure Statement is submitted:

a. ☐ within 3 months of the filing date of a national application other than a continued prosecution application under § 1.53(d);
☐ within 3 months of the date of entry of the national stage as set forth in § 1.491 in an International application;
☐ before the mailing date of a first Office Action on the merits; or
☒ before the mailing of a first Office Action after the filing of a request for continued examination under § 1.114.

b. ☐ after the events of above paragraph 1a and prior to the mailing date of a final Office Action or Notice of Allowance, and thus: ☐ the certification of paragraph 2 below is provided, or ☐ a fee of $180.00 is enclosed.

c. ☐ after the mailing date of a final Office Action or a Notice of Allowance and prior to payment of the issue fee, and thus: the certification of paragraph 2 below is provided and a fee of $180.00 is enclosed.

2. It is hereby certified:

☐ that each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the Statement, or

☐ that no item of information contained in the Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the person signing the certification after making reasonable inquiry, was known to any individual designated in § 1.56 (c) more than three months prior to the filing of the Statement.

3. ☐ Consideration of the following additional information (including any co-pending or abandoned U.S. applications, prior uses and/or sales, etc.) is requested:

4. For each non-English language reference listed on the attached Form PTO-1449:

☐ reference is made to an English language translation submitted herewith, and/or

☐ reference is made to a foreign patent office search report (in the English language) submitted herewith, and/or

☐ reference is made to an English language translation of a foreign patent office search report submitted herewith, and/or

☐ reference is made to the concise explanation contained in the specification of the present application at page(s) _____, and/or

☐ reference is made to the concise explanation set forth below:

5. ☐ Applicant also offers the following comments for the Examiner's consideration:

6. ☐ Also enclosed is a copy of a foreign search report citing these references.

7. ☐ The listed documents were brought to the attention of the Applicant(s) after payment of the issue fee in the captioned case. The documents were cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. Applicant(s) request this Information Disclosure Statement and attached Form PTO-1449 be placed in the file of the captioned application.

8. ☐ Applicant(s) requests that the Information Disclosure Statement and attached Form PTO-1449 and references, which are being filed before the grant of the patent and pursuant to 37 C.F.R. § 1.97(i), be placed in the file of the captioned application.

Applicant does not believe that any fees are required relating to this Information Disclosure Statement. If any required fees are missing, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert & Goetzel PC Deposit Account No. 50-1505/5150-63400/JCH.

Respectfully submitted,

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Date: 8/3/2005

Form PTO-1449 (modified) List of Patents and Publications For Applicant's Information Disclosure Statement (Use several sheets if necessary)	ATTY. DOCKET NO: 5150-63400	SERIAL NO: 10/055,691
	APPLICANT: Hugo A. Andrade	
	FILING DATE: October 29, 2001	GROUP: 2122

FOREIGN PATENT DOCUMENTS

EXAM. INITIALS	REF. DES	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION. YES/NO
	C1	WO 94 10627 A	5/11/94	PCT			
	C2	WO 94 15311 A	7/7/94	PCT			
	C3	DE 692 32 869 T2	Sept. 4, 2003	Germany			YES
	C4	DE 42 05 524 A1	Aug. 27, 1992	Germany			YES

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	C5	XP000554820 Edwards, et al., "Software acceleration using programmable hardware devices," IEEE Proceedings: Computers and Digital Techniques, vol. 143, no. 1, January 1996, pp. 55-63.
	C6	XP000380758 Lesser, et al, "High Level Synthesis and Generating FPGAs with the BEDROC System," Journal of VLSI Signal Processing, vol. 6, no. 2, August 1993, pp. 191-214.
	C7	Ade, M; Lauwereins, R; Peperstraete, J.A.; Hardware-Software Codesign with GRAPE, Proceedings of the Sixth IEEE International Workshop on Rapid System Prototyping, pp. 40-47, 6/9/95.
	C8	Lauwereins, R; Engels, M; Ade, M; Peperstraette, J; Grape-II: A System-Level Prototyping Environment for DSP Applications, Computer, Vol. 28, Issue 2, pp. 35-43, 2/95.
	C9	Lysaght, P; Stockwood, J; A Simulation Tool for Dynamically Reconfigurable Field Programmable Gate Arrays, IEEE Transactions on Very Large Scale Integration Systems, Vol. 4, Issue 3, pp. 381-390, 9/96.
	C10	De Coster, GRAPE-II: An Introduction [online]. Automatic Control and Computer Architectures Department. Katholieke Universiteit Leuven, Belgium, February 22, 1996 [retrieved October 6, 1999] Retrieved from the Internet @ http://www.esat.kuleuven.ac.be/acca
	C11	Weban et al., A Software Development System for FPGA-based Data Acquisition Systems, Proceedings of the IEEE Symposium on FPGAs for Custom Computing Machines, pp. 28-37, April 1996.
	C12	Petronino et al., An FPGA-based Data Acquisition System for a 95 GHz. W-band Radar, IEEE International Conference on Acoustics, Speech and Signal Processing, Vol. 5, pp. 4105-4108, April 1997.
	C13	Boulay et al., A High Throughput Controller for a 256-Channel Cardiac Potential Overlapping System, Canadian Conference on Electrical and Computer Engineering, Vol. 1, pp. 539-542, September 1995.
	C14	Collamati et al. "Induction Machine stator Fault On-line Diagnosis Based on LabVIEW Environment", Mediterranean Electrotechnical Conference, Vol. 1, pg. 495-498, May 1996.
	C15	Spoelder et al., "Virtual Instrumentation: A Survey of Standards and Their Interrelation", Proc. IEEE Instr. and Measurement Tech. Conf., Vol. 1, pp. 676-681, May 1997.

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	C16	Srinivasan et al., "LabVIEW program Design for On-Line Data Acquisition and Predictive Maintenance", Proc. Of the 30th Southeastern Symp. On System Theory, pp. 520-524, March 1998.
	C17	Wahidanabanu et al., "Virtual Instrumentation with Graphical Programming for Enhanced Detection and Monitoring of Partial Discharges", Proc. Electrical Insulation Conf. 1997, pp. 291-296, September 1997.
	C18	Choosing Block-Diagram Tools for DSP Design, http://www.bdti.com/articles/info_dspmt95blockdiagram.htm, May 9, 2003, pgs. 1-7.
	C19	Real-Time Workshop for Use with Simulink, User's Guide, May 1994, 229 pages.
	C20	Guide to Rapid Prototyping with Simulink, Real-Time Workshop and dSPACE, 1995, 16 pages.
	C21	Real-Time Interface to Simulink, RTI 30, User's Guide, 1995, 125 pages.
	C22	Kevin J Gorman and Kourosh J. Rahnamai, "Real-Time Data Acquisition and Controls Using MatLAB", 1995, 4 pages.
	C23	SPW – MatLAB Co-Simulation Interface Product Data Sheet, 1996, 2 pages.
	C24	Signal Processing WorkSystem, MatLAB Interface User's Guide, Oct. 1995, 72 pages.
	C25	Alta Group of Cadence Design Systems, Inc., 1995, 34 pages.
	C26	Code Generation System Product Data Sheet, 1994, 8 pages.
	C27	SPW/CGS Porting Kits Product Data Sheet, 11/94, 2 pages.
	C28	MultiProx for SPW Product Data Sheet, 08/94, 4 pages.
	C29	DSP ProCoder for SPW Product Data Sheet, 11/94, 4 pages.
	C30	Xanalog Corporation Sales Manual, January 1987, 8 pages.
	C31	Available XA-1000 Literature and Its Use, 1986, 2 pages.
	C32	Xanalog, XA-1000 Programming ICONS, 1986
	C33	Xanalog's CAE System: The Fastest AT Alive, Mass High Tech, Vol. 4, No. 22, 08/1988, 1 page.
	C34	Xanalog The Computer Aided Engineering Workstation Comes to Simulation, Simulation Vol. 47, No. 1, July 1986, 3 pages.
	C35	Xanalog RT Real Time Analog and Digital I/O, 10/90, 4 pages.
	C36	Xanalog/SC+, 9/90, 4 pages.
	C37	Xanalog Specializing in Workstations for Continuous Dynamic Simulation, 1987, 24 pages.
	C38	Xanalog Real-Time User Guide, 1994, 28 pages.

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	C39	Lee et al., "Gabriel: A Design Environment for Programmable DSPs", 11/7/1988, 13 pages.
	C40	Lee et al., "A Design Tool for Hardware and Software for Multiprocessor DSP Systems", May 1989, 4 pages.
	C41	Gabriel 0.7 Overview, 1990, 5 pages.
	C42	Joseph T. Buck and Edward A. Lee, "Scheduling Dynamic Dataflow Graphs with Bounded Memory Using the Token Flow Model", http://www.synopsys.com/, 1995, 4 pages.
	C43	Edward A. Lee, "Design Methodology for DSP", 1992, 4 pages.
	C44	Pino et al, "Interface Synthesis in Heterogeneous System-Level DSP Design Tools, 05/1996, 4 pages.
	C45	Jose Luis Pino, Master's Report, "Software Synthesis for Single-Processor DSP Systems Using Ptolemy", May 1993, 48 pages.
	C46	Asawaree Kalavade and Edward A. Lee, "A Hardware-Software Codesign Methodology for DSP Applications", 1993, 12 pages.
	C47	Pino et al., "Automatic Code Generation for Heterogeneous Multiprocessors", 1994, 4 pages.
	C48	Tool Chest continues to Grow, Electronic Engineering Times, 12/15/1995, 2 pages.
	C49	Pino et al., "Mapping Multiple Independent Syunchronous dataflow Graphs onto Heterogeneous Multiprocessors, 10/1994, 6 pages.
	C50	Asawaree Kalavade and Edward A. Lee, "Hardware/Software Co-Design Using Ptolemy – A Case Study, 09/1992, 18 pages.
	C51	Pino et al, "Software Synthesis for DSP Using Ptolemy", 1995, 15 pages.
	C52	Vol. 1 – Ptolemy 0.7 User's Manual, 1997, 532 pages.
	C53	i-Logix Product Overview, 1996, 52 pages.
	C54	Press Release, i-Logix Statemate MAGNUM Supports PCs", 01/31/1997, 2 pages.
	C55	Press Release, "i-Logix Signs Reseller Agreement for Virtual Prototypes, Inc.'s VAPS Product Line, 02/11/1997, 2 pages.
	C56	Press Release, "i-Logix Introduces Rhapsody, Object-Oriented analysis, Design and Implementation Tool", 02/10/1997, 2 pages.
	C57	Statemate/C Product Overview, 1995, 4 pages.
	C58	Press Release, "i-Logix and Integrated Systems Link Statemate MAGNUM and MATRIX AutoCode" 01/03/1997, 2 pages
	C59	Press Release, "i-Logix and Wind River unveil Industry's First Rapid Prototyping Solution for Testing Embedded Systems at ESC West in San Jose, 09/17/1996, 3 pages.
	C60	Press Release, "i-Logix Inc. Endorses Unified Modeling Language, 01/16/1997, 1 page.

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	C61	Levy, M., "DSP Design Tools Target FPGAs," www.reed-electronics.com/ednmag/archives/1996/062096/13df2.htm, June 20, 1996.
	C62	Heimdahl, M.P.E., Keenan, D.J., "Generating Code from Hierarchical State-Based Requirements," Proceedings of IEEE International Symposium on Requirements Engineering (RE'97)," January 1997.
	C63	Integrated Systems, Inc., "MATRIXx Product Family Technical Specifications," Product Manual, Copyright 1995.
	C64	Pauer, E.K., "Multiprocessor System Development for High Performance Signal Processing Applications," Proceedings of the 1997 IEEE Int. Workshop on Rapid System Prototyping (RSP)," Copyright 1997.
	C65	Drusinsky, D., "Extended State Diagrams and Reactive Systems," Dr. Dobb's Journal, October 1994.
	C66	Ade, M., Lauwereins, R., and Peperstraete, J.A., "Hardware-Software Codesign with GRAPE," Rapid System Prototyping, Proceedings of the Sixth IEEE International Workshop on Rapid System Prototyping (RSP'95), 1995.
	C67	Chen, X., Ling, X., Amano, H., "Software Environment for WASMII: a Data Driven Machine with a Virtual Hardware," Proceedings of 4th Workshop on Field-Programmable Logic and Applications (FPL '94), pages 208-219, Springer Verlag, September 1994.

EXAMINER:	DATE CONSIDERED:

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the patent owner.